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None

(58) Field of Search
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ONLINE: WPI, EPODOC, JAPIO

(54) Abstract Title
METHOD FOR FORMING AN ELECTRONIC STRUCTURE

(57) A method for forming an electronic structure comprises removing a portion of a dielectric layer from a substrate 52 to form a void 56. The void portion 56 may completely or partly surround a second portion 57 of the dielectric layer. A conductive pad 54 is formed on the second portion 57 of dielectric. The void may be formed using a laser. The method and structure may be used to reduce thermally induced strains on solder joints 48 that couple a ball grid array (BGA) module 40 to a circuit card 50.

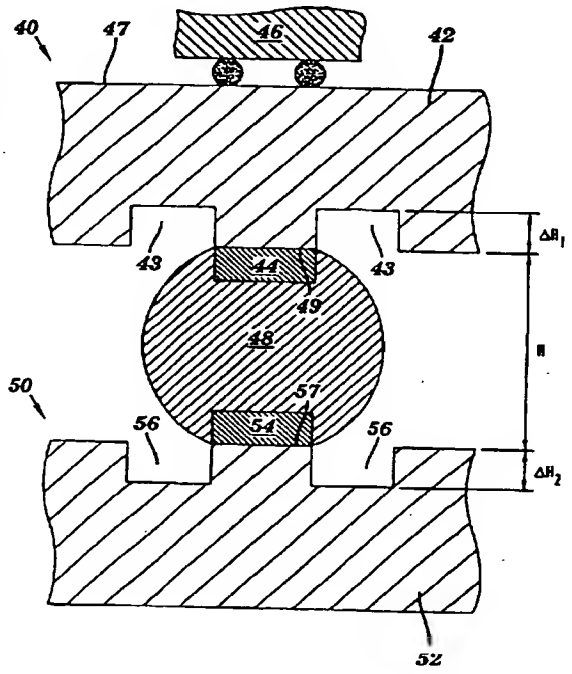

FIG. 2

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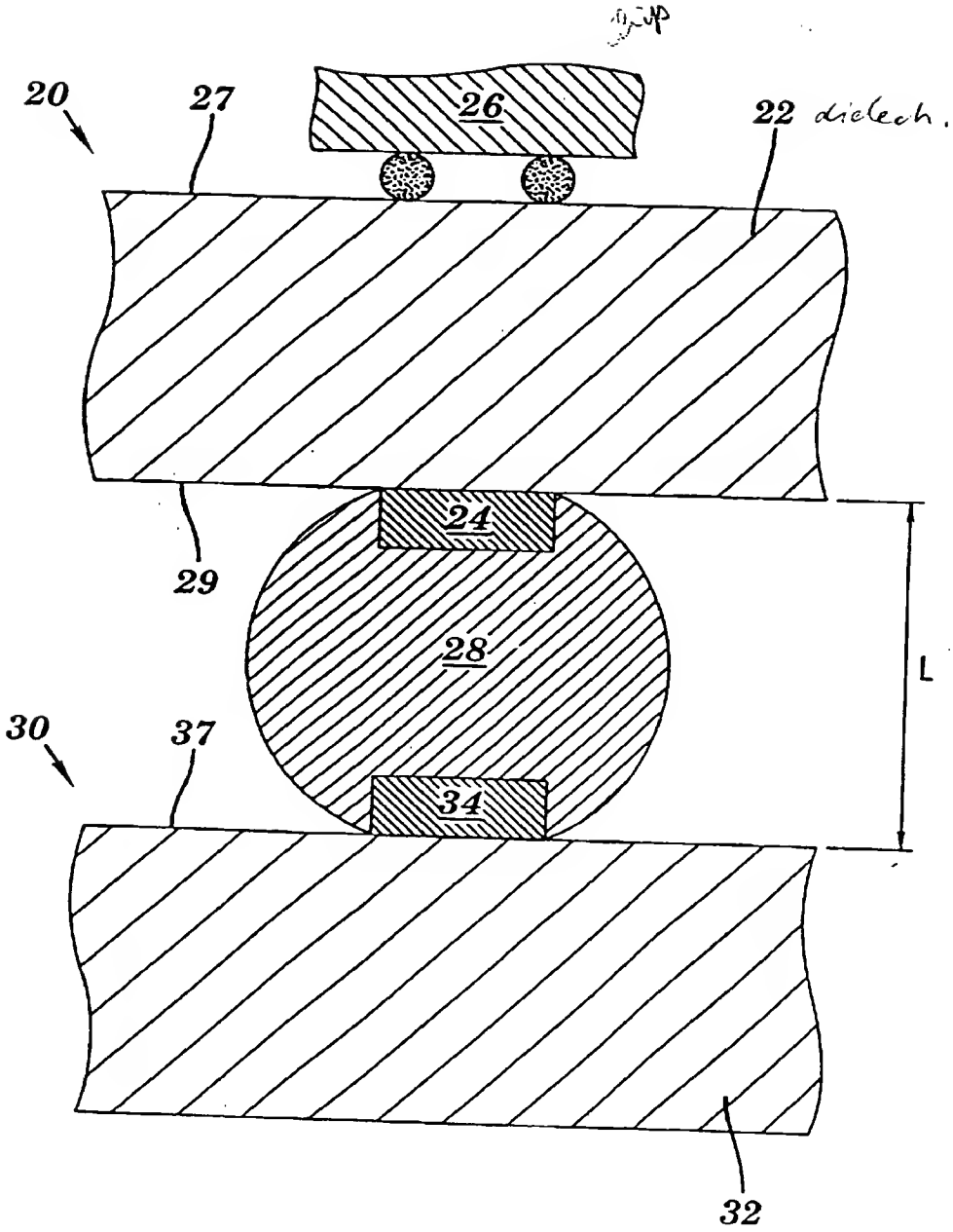

FIG. 1

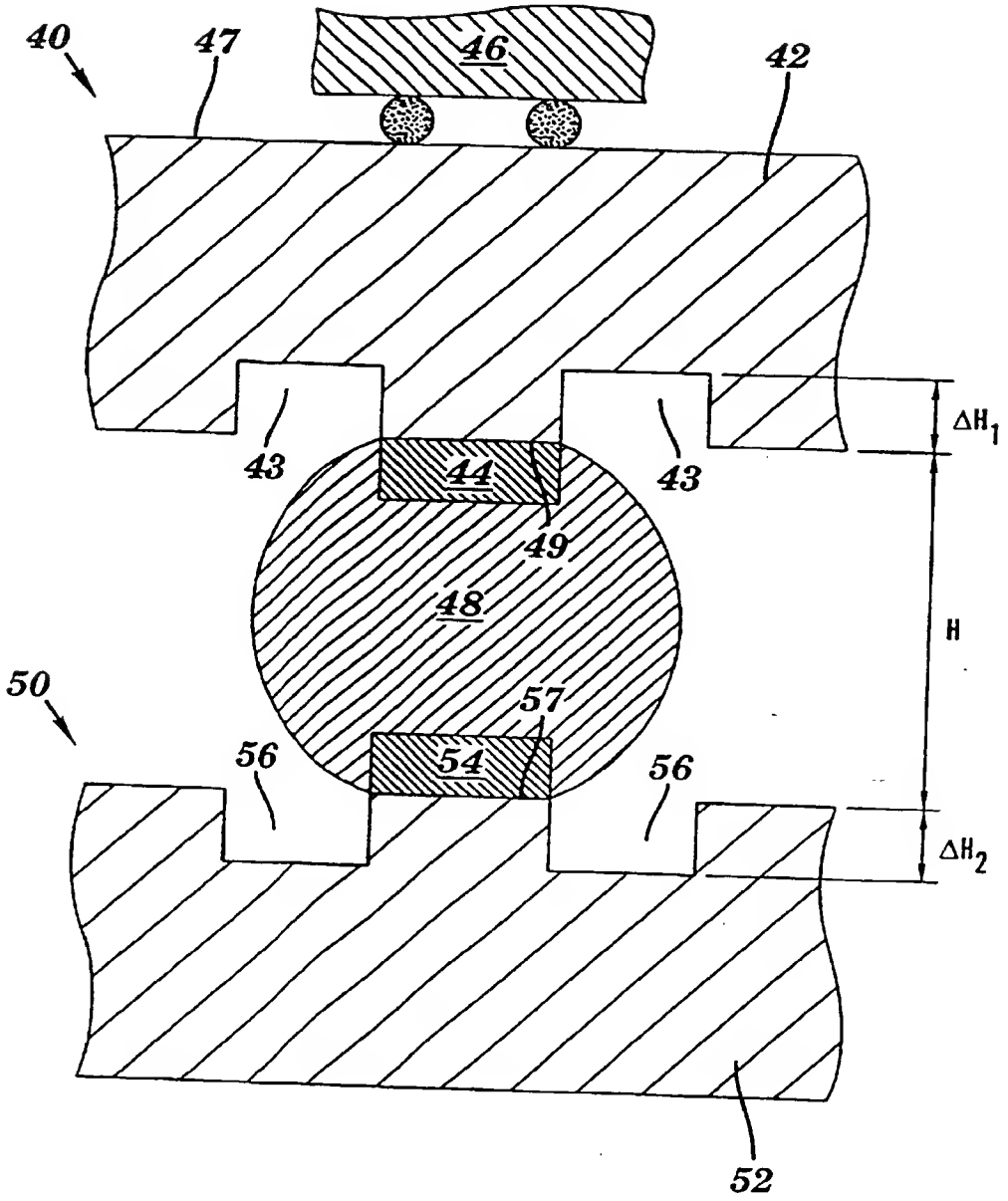

FIG. 2

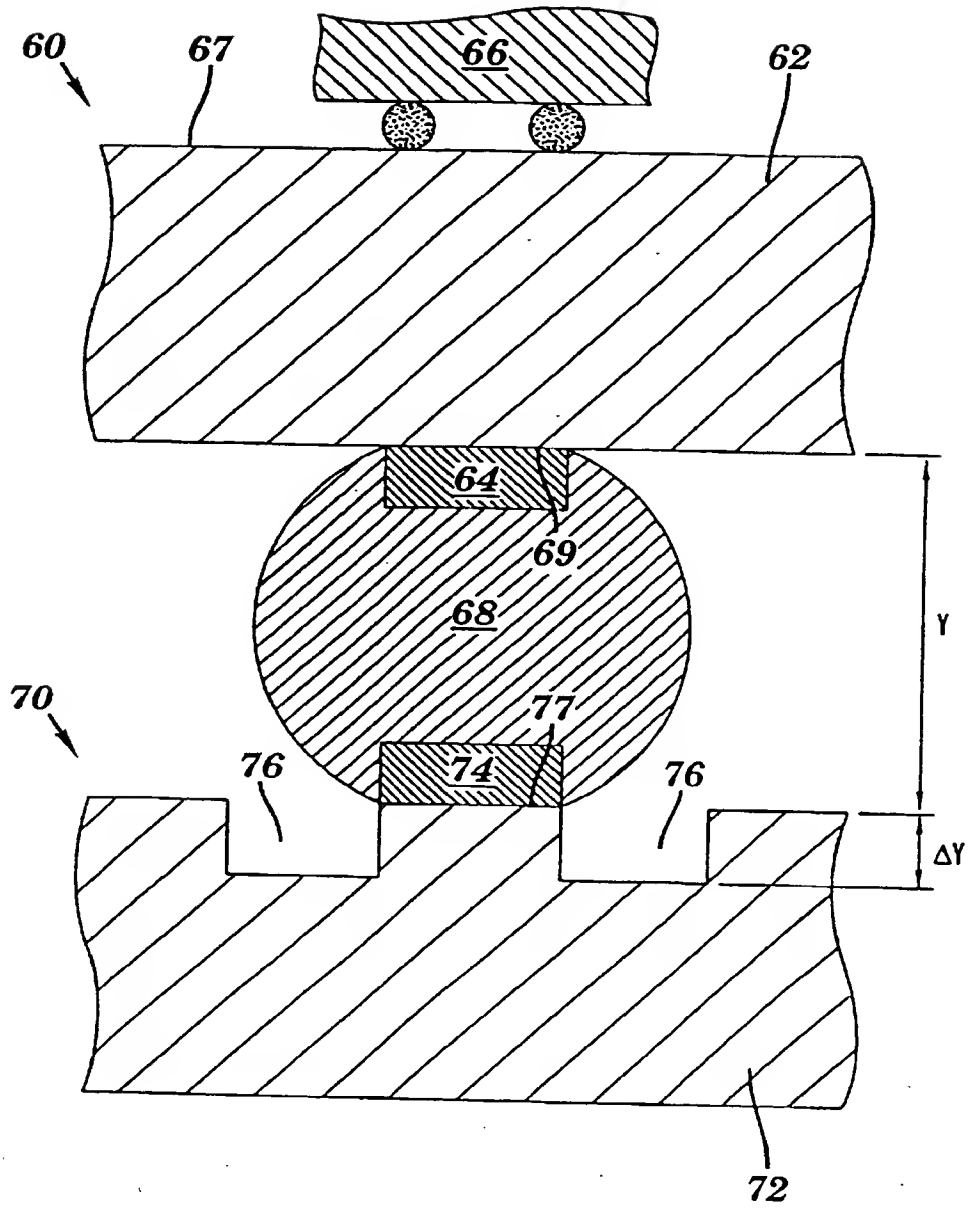

FIG. 3

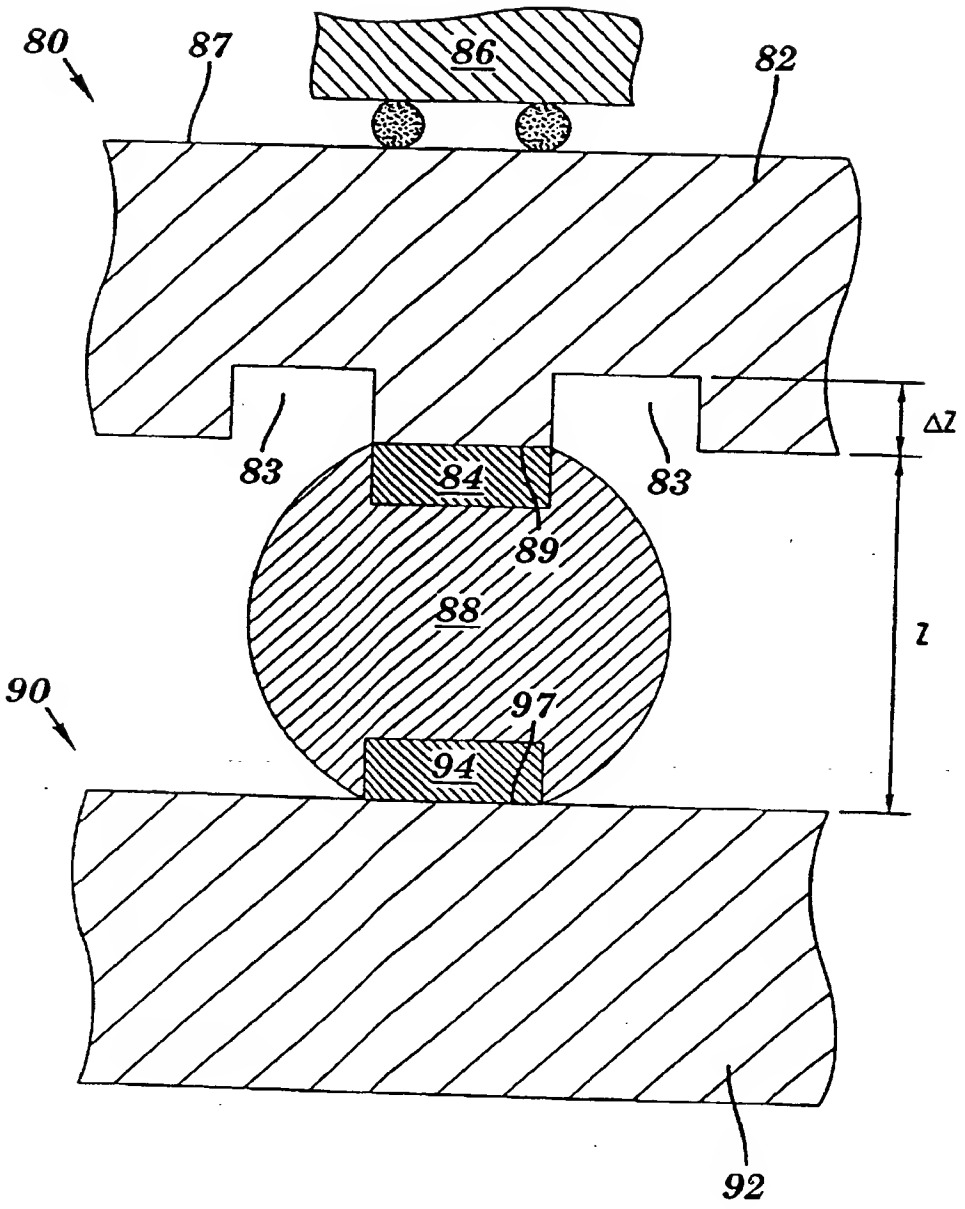

FIG. 4

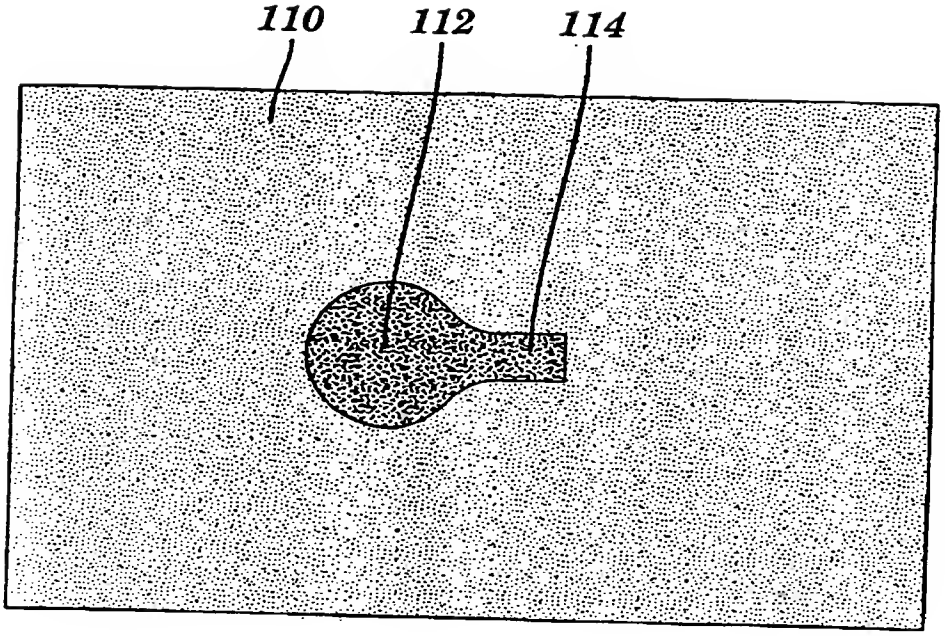

FIG. 5

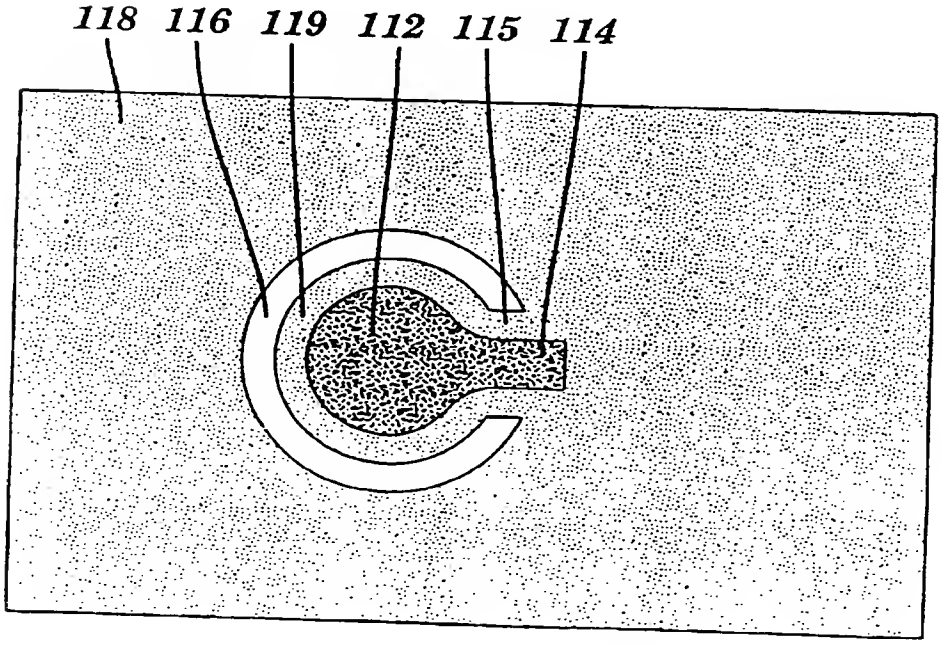

FIG. 6

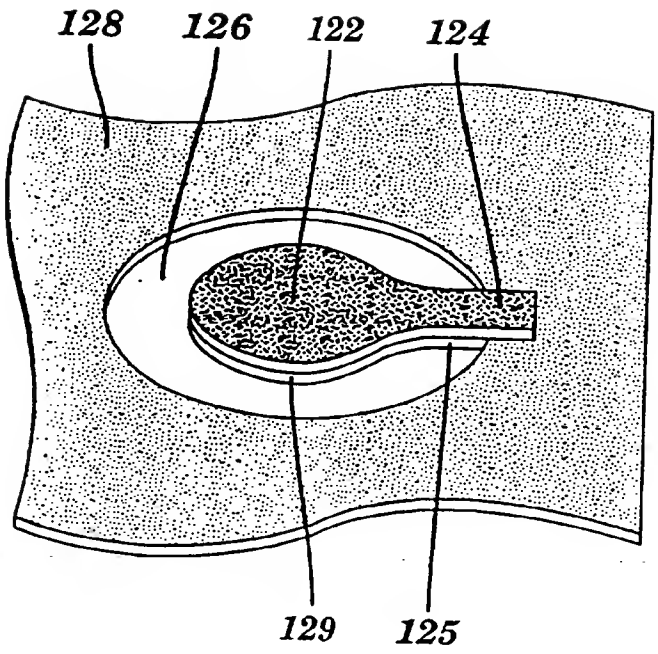

FIG. 7

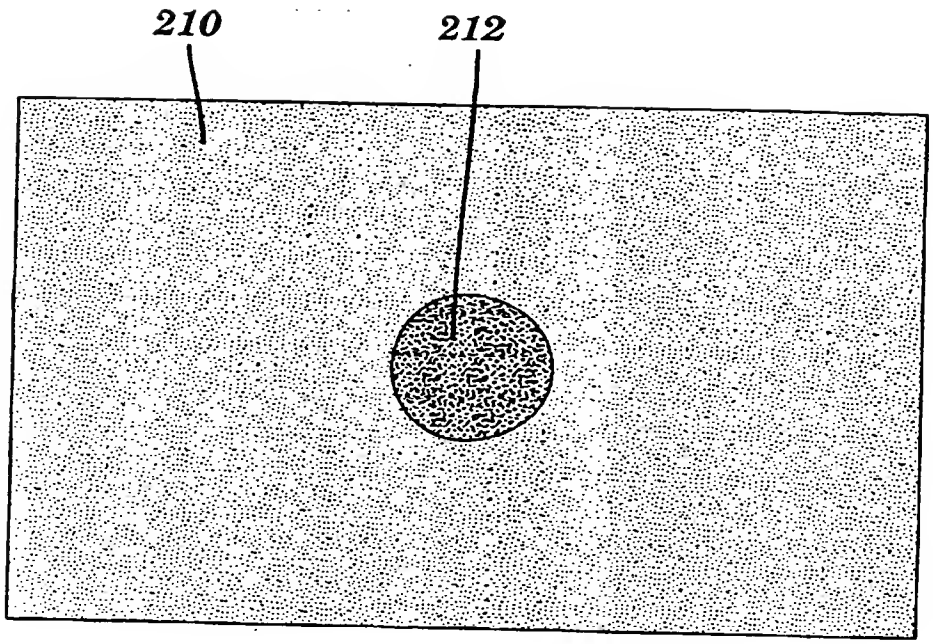

FIG. 8

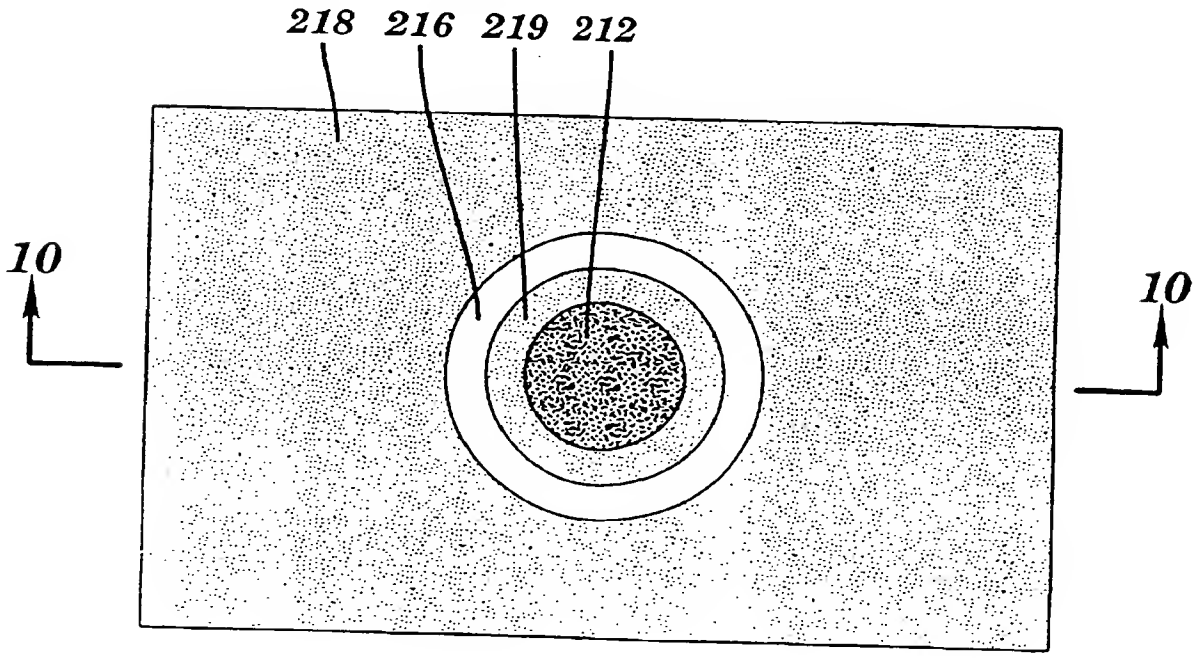

FIG. 9

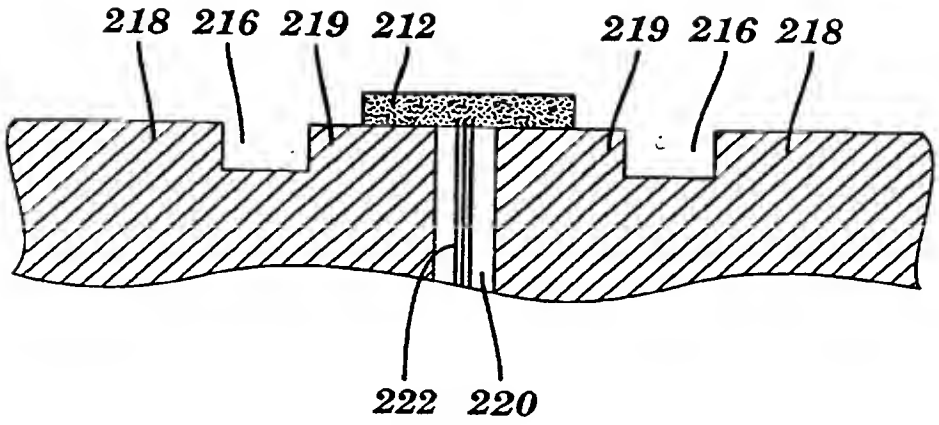

FIG. 10

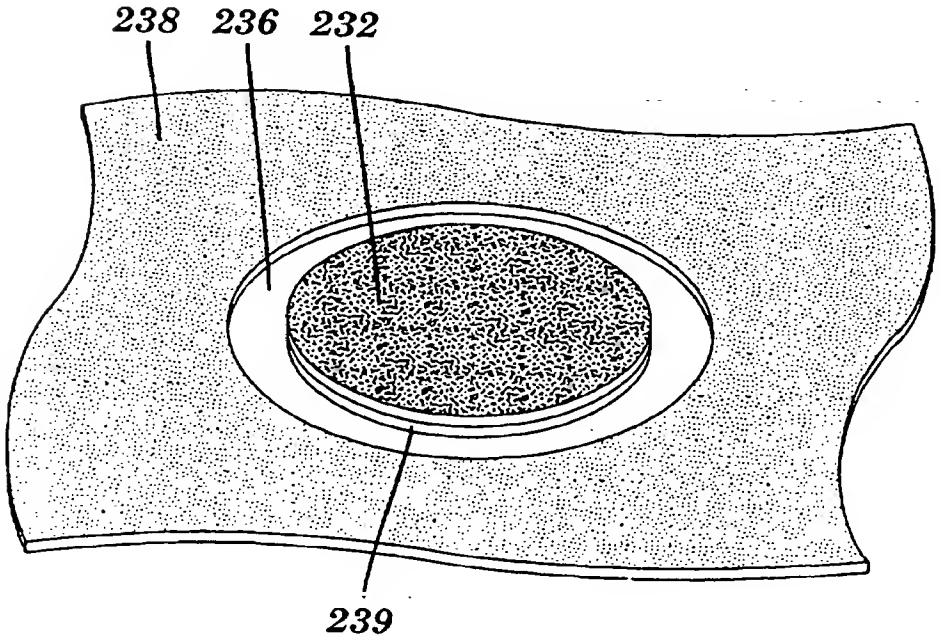

FIG. 11

METHOD AND STRUCTURE FOR REDUCING STRAINS IN SOLDER JOINTS

The present invention relates to a structure and associated method of fabrication for reducing thermally induced strains in solder joints associated with solder balls that couple a substrate (e.g. ball grid array (BGA) module) to a circuit card.

A contemporary circuit board configuration may have a BGA module mounted on a circuit card. A BGA module comprises a substrate of dielectric material, such as ceramic or plastic, having both a top surface and a bottom surface. An array of solder balls are attached to a corresponding array of conductive pads on the bottom side of the BGA module, while one or more chips are attached to the top side of the BGA module. The pertinent circuit card is any pre- wired board comprising dielectric material and an array of conductive pads on the board. An example of a circuit card is a motherboard of a computer. The circuit card pads serve as attachment points for accommodating one or more BGA modules. Accordingly, a BGA module that is mounted on a circuit board has each solder ball attached to a conductive pad on the BGA module itself and also to a conductive pad on the circuit card. These conductive pads are respectively affixed to the dielectric substrate of the BGA module and the dielectric board of the circuit card. Thus, each solder ball is a structural element that is mechanically attached to dielectric sheets of material on each side of the solder ball.

When the circuit card is heated or cooled, the solder ball is subject to strains that arise from the differential rate of thermal expansion of the supporting dielectric structures. For example, a typical thermal expansion coefficient of the circuit card is 14 to 22 ppm/°C (ppm denotes parts per million), while a ceramic substrate of a BGA module may have a smaller thermal expansion coefficient of approximately 6 to 11 ppm/°C. If the BGA module uses a plastic substrate material, the effective thermal expansion coefficient of the plastic substrate, at locations where a silicon chip constrains expansion of the substrate, is typically about 7 ppm/°C . While the preceding materials, and corresponding thermal expansion coefficients, typify BGA substrates and circuit cards, materials could be characterized by a reversed relationship in which the BGA substrate has a higher thermal expansion coefficient than that of the circuit card to which the BGA module is attached.

Unfortunately, strains on the solder balls resulting from the aforementioned differential thermal expansion may cause fatigue failure in the BGA solder joints. U.S. Pat. 5,726,079 (Johnson, 3/10/98), which is hereby incorporated by reference, discloses an approach that could be used to reduce the effect of differential thermal expansion. With this alternative approach, a chip mounted on a substrate is encased peripherally with a dielectric material that is mechanically bonded to the substrate. Additionally, the chip is mechanically coupled to a conductive plate located above the top side of the chip, wherein the conductive plate comprises a material such as a stainless steel. Because of the mechanical bonding between the conductive plate and the substrate through the encased dielectric material, bending of the structure due to the differential thermal expansion is eliminated and the thermal expansion of the conductive plate mitigates the thermal expansion of the substrate of the BGA module. Thus the material of the conductive plate would be selected to have a thermal expansion coefficient that would eliminate the bending that arises from the mismatched thermal expansions of the substrate of the BGA module and the dielectric board of the circuit card. Although this method would greatly extend the BGA fatigue life, it would also increases the product's cost because of the cost of the conductive plate and because of the process steps and associated equipment required to fabricate the encasing structure.

The present invention provides an inexpensive method, and an associated electrical structure, that reduces the thermally induced strain on solder balls of BGA modules, wherein the BGA module is mounted on a circuit card. The essence of the method is to increase the effective length of the connecting structure, between the BGA module and the circuit card, that deforms due to differential thermal expansion. This results in a reduction in strain in the connecting structure and, in particular, in the solder ball. Thus, increasing the length over which a given displacement acts effectively reduces the strain throughout the solder ball. In particular, the method of the present invention forms annular voids by removing material from the dielectric substrate of the BGA module so as to leave the solder balls affixed to regions of dielectric material, wherein the regions of dielectric material are each substantially surrounded by an annular void thus formed. Annular voids may be similarly formed around the regions of the dielectric board of the circuit card, wherein the regions are underneath the conductive pads of the circuit card to which the BGA module will be attached. Thus, the method forms peninsulas of dielectric regions if the formed annular voids substantially,

but not completely, surround the dielectric regions. Alternatively, the method forms islands of dielectric regions if the formed annular voids totally surround the dielectric regions. A peninsula thus formed will be unseparated from the remaining dielectric substrate (or board), thereby leaving a thin connecting dielectric strip between the peninsula and the remaining dielectric substrate (or board).

According to one aspect, the present invention provides a method for forming at least one electrical structure, comprising the steps of: providing a substrate including a dielectric layer having a first surface, and at least one electrically conductive pad attached to the first surface; and removing a first portion of the dielectric layer to form a void portion of the dielectric layer, wherein the void portion substantially surrounds a second portion of the dielectric layer, and wherein the pad is positioned on the second portion.

According to a second aspect, the present invention generally provides at least one electrical structure, comprising: a substrate including a dielectric layer having a first surface; at least one electrically conductive pad attached to the first surface; and a void portion of the dielectric layer, wherein the void portion substantially surrounds a second portion of the dielectric layer, and wherein the pad is positioned on the second surface.

The present invention has several advantages. The present invention protects the integrity of solder joints to extend the fatigue life of BGA modules. The method of the present invention is inexpensive compared with other methods, such as that of U.S. Pat. 5,726,079, discussed above. Moreover, the present invention does not preclude using other methods and could be used in conjunction with other methods with little added cost.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIG. 1 depicts a front cross-sectional view of a BGA module attached to a circuit card;

FIG. 2 depicts a front cross-sectional view of a BGA module attached to a circuit card, with void regions surrounding dielectric material under both the BGA pad and the circuit card pad;

FIG. 3 depicts a front cross-sectional view of a BGA module attached to a circuit card, with a void region surrounding dielectric board material under the circuit card pad;

FIG. 4 depicts a front cross-sectional view of a BGA module attached to a circuit card, with a void region surrounding dielectric substrate material under the BGA pad;

FIG. 5 depicts a top view of a substrate having a pad with a connecting strip;

FIG. 6 depicts FIG. 5 with a void region substantially, but not totally, surrounding dielectric material underneath the pad;

FIG. 7 depicts a top perspective view of a substrate with a void region substantially, but not totally, surrounding dielectric material underneath a pad on the substrate;

FIG. 8 depicts a top view of a substrate having a pad;

FIG. 9 depicts FIG. 8 with a void region surrounding dielectric material underneath the pad;

FIG. 10 depicts a cross-sectional side view of the configuration of FIG. 9, showing a wiring pattern that is routed to the pad; and

FIG. 11 depicts a top perspective view of a substrate with a void region totally surrounding dielectric material underneath a pad on the substrate.

FIG. 1 illustrates a front cross-sectional view of a BGA module 20 attached to a circuit card 30. The BGA module 20 comprises a dielectric substrate 22, a chip 26 attached to a top side 27 of the substrate 22, a BGA pad 24 attached to a bottom side 29 of the substrate 22, and a solder ball 28 of height L attached to the BGA pad 24. The circuit card 30 comprises a dielectric board 32 and a circuit card pad 34 attached to a top side 37 of the board 32. The circuit card may be any pre-wired board comprising dielectric material, such as a motherboard of a computer. The solder ball 28 is attached to pad 34 on circuit card 30, thereby connecting the BGA module 20 to the circuit card 30. The thermally induced strain on the solder ball 28 generated during thermal cycles are distributed over the

height L. The intent of the present invention is to modify the substrate 22 and/or the board 32 so as to redistribute the strain over a height greater than L in order to increase the fatigue life of the configuration of FIG. 1.

FIG. 2 illustrates an embodiment of the present invention that increases the effective height over which the strain is distributed when compared with the configuration of FIG. 1. FIG. 2 shows a front cross-sectional view of a BGA module 40 attached to a circuit card 50. The BGA module 40 comprises a dielectric substrate 42, a chip 46 attached to a top side 47 of the substrate 42, a BGA pad 44 attached to a bottom side 49 of the substrate 42, and a solder ball 48 of height H is attached to the BGA pad 44. The circuit card 50 comprises a dielectric board 52 and a circuit card pad 54 attached to a top side 57 of the board 52. The solder ball 48 is attached to the circuit card pad 54, thereby connecting the BGA module 40 to the circuit card 50. An annular void 43 of height ΔH_1 within the substrate 42 surrounds substrate material underneath the BGA pad 44. An annular void 56 of height ΔH_2 within the board 52 surrounds board material underneath the circuit card pad 54. Without the annular voids 43 and 56, the thermally induced strain would be distributed over height H in accordance with the prior art. With the annular voids 43 and 56 of Fig. 2, however, the deformation is distributed over the greater height $H+\Delta H_1+\Delta H_2$ thereby reducing the strain throughout the solder ball 48. The annular voids 43 and 56 respectively provide space so that the substrate material underneath the BGA pad 44 and the board material underneath the circuit card pad 54 are less constrained, thereby increasing their compliance and alleviating the thermally induced strain in the solder ball 48.

FIG. 3 illustrates an embodiment of the present invention that increases the effective height over which thermal strain is distributed relative to the configuration of FIG. 1. FIG. 3 shows a front cross-sectional view of a BGA module 60 attached to a circuit card 70. The BGA module 60 comprises a dielectric substrate 62, a chip 66 attached to a top side 67 of the substrate 62, a BGA pad 64 attached to a bottom side 69 of the substrate 62, and a solder ball 68 of height Y that is attached to the BGA pad 64. The circuit card 70 comprises a dielectric board 72 and a circuit card pad 74 attached to a top side 77 of the board 72. The solder ball 68 is attached to the circuit card pad 74, thereby connecting the BGA module 60 to the circuit card 70. An annular void 76 of height ΔY within the board 72 surrounds board material underneath the circuit card pad 74. Without the annular void 76, the thermally induced strain would be

distributed over height Y in accordance with the prior art. With the annular void 76 of Fig. 3, however, the deformation is distributed over the greater height $Y+\Delta Y$, thereby reducing the strain throughout the solder ball 68. The annular void 76 provides space so that the substrate material underneath the circuit card pad 74 is less constrained, thereby increasing its compliance and alleviating the thermally induced strain in the solder ball 68.

FIG. 4 illustrates an embodiment of the present invention that increases the effective height over which strain is distributed when compared with the configuration of FIG. 1. FIG. 4 shows a front cross-sectional view of a BGA module 80 attached to a circuit card 90. The BGA module 80 comprises a dielectric substrate 82, a chip 86 attached to a top side 87 of the substrate 82, a BGA pad 84 attached to a bottom side 89 of the substrate 82, and a solder ball 88 of height Z that is attached to the BGA pad 84. The circuit card 90 comprises a dielectric board 92 and a circuit card pad 94 attached to a top side 97 of the board 92. The solder ball 88 is attached to the circuit card pad 94, thereby connecting the BGA module 80 to the circuit card 90. An annular void 83 of height ΔZ within the substrate 82 surrounds substrate material underneath the BGA pad 84. Without the annular void 83, the thermally induced strain is distributed over height Z in accordance with the prior art. With the annular void 83 of Fig. 4, however, the thermal shear stresses are distributed over the greater height $Z+\Delta Z$, thereby reducing the strain throughout the solder ball 88. The annular void 83 provides space so that the substrate material underneath the circuit card pad 84 is less constrained, thereby increasing its compliance and alleviating the thermally induced strain in the solder ball 88.

If an annular void in FIGS. 2-4 substantially but not totally surrounds dielectric material underneath a pad, a peninsula of dielectric material under the pad will have been defined by the annular void. Alternatively, if an annular void in FIGS. 2-4 totally surrounds dielectric material underneath a pad, an island of dielectric material under the pad will have been defined by the annular void.

FIGS. 5-7 illustrate a process according to an embodiment of the present invention which forms an annular void that substantially but not totally surrounds dielectric material under a pad to create a peninsula of dielectric material. The process begins with the configuration of FIG. 5, which shows a top view of a pad 112 on a substrate 110 with a wiring

pattern 114 that is attached to the pad 112. The substrate 110 represents either a dielectric substrate of a BGA module, or a dielectric board of a circuit card, as described for FIGS. 1-3. Next, FIG. 6 shows the result of forming an annular void 116 that substantially but not totally surrounds dielectric material underneath the pad 112. As a result, a peninsula 119 of dielectric material is created under the pad 112, wherein a strip 115 of dielectric substrate material connects the peninsula 119 to the remainder 118 of the substrate 110 (see FIG. 5 for substrate 110). The strip 115 serves to mechanically support the wiring pattern 114, which electrically couples the pad 112 to the substrate 110 or to internal circuitry of the BGA module or circuit card that comprises the substrate 110.

The peninsula 119 is shown in FIG. 6 to comprise a larger area than the area of pad 112 which rests on the peninsula 119. FIG. 7 shows a perspective view of an alternative configuration of a substrate 128 with an annular void 126 that substantially but not totally surrounds a peninsula 129 of substrate material, wherein the area of the peninsula 129 is approximately the same as the area of the pad 122 that rests on the peninsula 129. A strip 125 of dielectric substrate material connects the peninsula 129 to the substrate 128 and serves to mechanically support a wiring pattern 124 that is attached to the pad 122. The wiring pattern 124 electrically couples the pad 122 to the substrate 128 or to internal circuitry of the BGA module or circuit card that comprises the substrate 128.

FIGS. 8-11 illustrate, according to another embodiment, a process of the present invention which forms an annular void that totally surrounds dielectric material under a pad to create an island of dielectric material. The process begins with the configuration of FIG. 8, which shows a top view of a pad 212 on a substrate 210. The substrate 210 represents either a dielectric substrate of a BGA module, or a dielectric board of a circuit card, as described for FIGS. 1-3. Next, FIG. 9 shows the result of forming an annular void 216 that totally surrounds dielectric material underneath the pad 212. As a result, an island 219 of dielectric material is created under the pad 212, leaving a remainder 218 of the substrate 210 (see FIG. 8 for substrate 210). FIG. 10 illustrates a cross-sectional view of the configuration of FIG. 9, showing a wiring pattern 222 within a via 220, wherein the via 220 is contained within the island 219. The wiring pattern 222 is routed upward to connect the pad 212 with internal circuitry of the BGA module or circuit card that comprises the substrate 210.

The island 219 is shown in FIG. 9 to comprise a larger area than the area of pad 212 which rests on the island 219. FIG. 11 shows a perspective view of an alternative configuration of a substrate 238 with an annular void 236 that totally surrounds an island 239 of substrate material, wherein the area of the island 239 is approximately the same as the area of the pad 232 that rests on the island 239. There is a wiring pattern (not shown) similar to that in FIG. 10, wherein the wiring pattern is within a via that is contained within the island 239, and wherein the wiring pattern is routed upward to connect the pad 232 with internal circuitry of the BGA module or circuit card that comprises the substrate 238.

The annular voids of FIGS. 2-11 may be formed by any method known to those of ordinary skill in the art. In particular, the annular voids my be formed by laser ablation using any one of various types of lasers as are known to those skilled in the art. A practical laser for this purpose is a frequency tripled Neodymium YAG laser using ultraviolet emission, high peak power, high repetition rate, and a focused beam of 6 to 50 μm in diameter. Generally, dielectric polymers absorb best at ultraviolet energies and the thermal damage to the nonablated portions is minimal. A useful wavelength in the ultraviolet range is 355 nm. Because the areas to be scanned are usually larger than the beam size, a raster scan may be created to cover the area to be scanned. Scan spacing is typically 80% of the spot size in order to provide some overlap of the guassian beam. Depending on the material, repetition rates of 1,000 Hz to 20,000 Hz can be utilized, with the 1,000 Hz rate providing the highest power per pulse of 12KW which drops to 0.5 KW at 20,000 Hz. An example of a specific process is ablating a circular pad on a carrier made of a glass-cloth reinforced epoxy material such as FR-4, with a 14 μm beam scanned over the target area at 2,000Hz, 8.3 KW per pulse, and a pulse spacing of 11 μm. Each scan pass removes approximately 20 μm of material. To remove 200 μm (0.008 inch), 10 scan passes would be needed. As an alternative to the preceding Neodymium YAG laser, other laser technologies (e.g., CO_2 and Excimer) can be used to achieve similar results.

Although the preferred embodiments described herein pertain to annular void regions surrounding dielectric matter underneath a pad on a BGA module or on a circuit card, the present invention applies to any configuration having annular void regions surrounding dielectric matter underneath a pad on a dielectric substrate.

While preferred and particular embodiments of the present invention have been described herein for purposes of illustration, many modifications

and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the scope of this invention.

CLAIMS

1. A method for forming an electrical structure, comprising the steps of:

providing a substrate including a dielectric layer having a first surface, and at least one electrically conductive pad attached to the first surface; and

removing a first portion of the dielectric layer to form a void portion of the dielectric layer, wherein the void portion substantially surrounds a second portion of the dielectric layer, and wherein the pad is positioned on the second portion.

2. The method of claim 1, wherein the removing step is accomplished by using a laser.

3. The method of claim 1, wherein the removing step results in a strip of the dielectric layer connecting the second portion to a remaining portion of the dielectric layer.

4. The method of claim 1, wherein the removing step results in the second portion being unconnected to a total remaining portion of the dielectric layer.

5. The method of claim 3, wherein the providing step further comprises providing an internal wiring pattern that is electrically connected to the pad, and wherein the removing step results in the strip being underneath a portion of the internal wiring pattern.

6. The method of claim 4, wherein the providing step further comprises providing an internal wiring pattern that is electrically connected to the pad, and wherein a portion of the internal wiring pattern is contained within a via that is located underneath the pad.

7. The method of claim 1, wherein the providing step further comprises providing an internal wiring pattern that is electrically connected to the pad, and wherein the removing step does not remove any portion of the internal wiring pattern.

8. The method of claim 7, further comprising the following steps for forming a ball grid array module:

providing a solder ball;

attaching the solder ball to the pad; and

affixing a chip to a second surface of the dielectric layer, wherein the chip is electrically connected to the internal wiring pattern.

9. The method of claim 8, wherein the affixing step is performed prior to the attaching step.

10. The method of claim 8, further comprising fastening the ball grid array module to a circuit card.

11. The method of claim 8, further comprising:

forming a first electrical structure of the at least one electrical structure, wherein the providing step provides a first pad of the at least one electrically conductive pad; and

affixing the ball grid array module to the first electrical structure by affixing the solder ball to the first pad.

12. The method of claim 11, wherein the forming of the first electrical structure precedes the forming of the ball grid array module.

13. An electrical structure, comprising:

a substrate including a dielectric layer having a first surface;

at least one electrically conductive pad attached to the first surface; and

a void portion of the dielectric layer, wherein the void portion substantially surrounds a second portion of the dielectric layer, and wherein the pad is positioned on the second surface.

14. The electrical structure of claim 13, wherein a strip of the dielectric layer connects the second portion to a remaining portion of the dielectric layer.

15. The electrical structure of claim 13, wherein the second portion is unconnected to a total remaining portion of the dielectric layer.

16. The electrical structure of claim 14, further comprising an internal wiring pattern that is electrically connected to the pad, wherein the strip is underneath a portion of the internal wiring pattern.

17. The electrical structure of claim 15, further comprising an internal wiring pattern that is electrically connected to the pad, wherein a portion of the internal wiring pattern is contained within a via that is located underneath the pad.

18. The electrical structure of claim 13, further comprising an internal wiring pattern that is electrically connected to the pad.

19. The electrical structure of claim 18, wherein the electrical structure is a ball grid array module such that the electrical structure further comprises:

a solder ball attached to the pad; and

a chip attached to a second surface of the dielectric layer, wherein the chip is electrically connected to the internal wiring pattern.

20. The electrical structure of claim 19, further comprising the ball grid array module affixed to a circuit card.

21. The electrical structure of claim 19, further comprising:

a first electrical structure of the at least one electrical structure, wherein the first electrical structure comprises a first pad of the at least one electrically conductive pad, and wherein the ball grid array module is affixed to the first electrical structure such that the solder ball is affixed to the first pad.

INVESTOR IN PEOPLE

Application No: GB 0004103.8 **Examiner:** Claire Williams
Claims searched: all **Date of search:** 3 August 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K (KRG)

Int Cl (Ed.7): H01L 23/485, 23/488 H05K 3/34

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	NONE	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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